W39V040B Data Sheet

512K × 8 CMOS FLASH MEMORY WITH LPC INTERFACE

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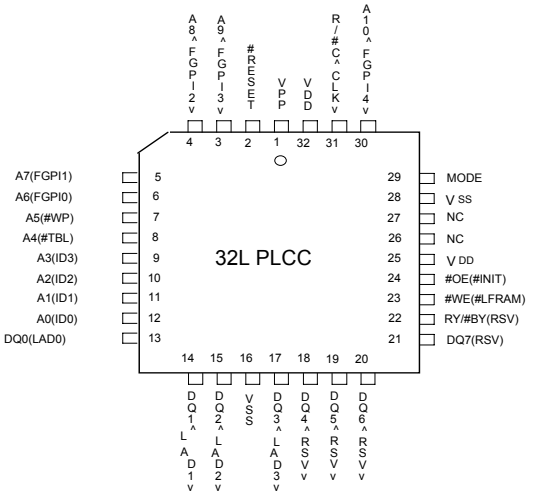
1. GENERAL DESCRIPTION

The W39V040B is a 4-megabit, 3.3-volt only CMOS flash memory organized as 512K × 8 bits. For flexible erase capability, the 4Mbits of data are divided into 8 uniform sectors of 64 Kbytes. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is required for accelerated program. The unique cell architecture of the W39V040B results in fast program/erase operations with extremely low current consumption. This device can operate at two modes, Programmer bus interface mode, Low pin count (LPC) bus interface mode. As in the Programmer interface mode, it acts like the traditional flash but with a multiplexed address inputs. But in the LPC interface mode, this device complies with the Intel LPC specification. The device can also be programmed and erased using standard EPROM programmers.

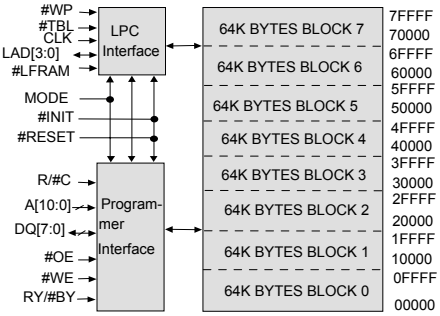
2. FEATURES

- Single 3.3-volt operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast Program operation:
  - Byte-by-Byte programming: 9 μS (typ.) (V_{PP} = 12V)
  - Byte-by-Byte programming: 12 μS (typ.) (V_{PP} = Vcc)
- Fast Erase operation:
  - Sector erase 0.6 Sec. (typ.)
- Fast Read access time: Tkq 11 nS
- Endurance: 10K cycles (typ.)
- Twenty-year data retention
- 8 Even sectors with 64K bytes
- Any individual sector can be erased
- Hardware protection:
  - #TBL supports 64-Kbyte Boot Block hardware protection
  - #WP supports the whole chip except Boot Block hardware protection
- Low power consumption
  - Active current: 15 mA (typ. for LPC read mode)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32L PLCC, 32L STSOP
  32L PLCC Lead free, 32L STSOP Lead free

3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYM.	INTERFACE		PIN NAME
	PGM	LPC	
MODE	*	*	Interface Mode Selection
#RESET	*	*	Reset
#INIT		*	Initialize
#TBL		*	Top Boot Block Lock
#WP		*	Write Protect
CLK		*	CLK Input
FGPI[4:0]		*	General Purpose Inputs
ID[3:0]		*	Identification Inputs They Are Internal Pull Down to Vss
LAD[3:0]		*	Address/Data Inputs
#LFRAM		*	LPC Cycle Initial
R/#C	*		Row/Column Select
A[10:0]	*		Address Inputs
DQ[7:0]	*		Data Inputs/Outputs
#OE	*		Output Enable
#WE	*		Write Enable
RY/#BY	*		Ready/ Busy
VDD	*	*	Power Supply
VSS	*	*	Ground
VPP	*	*	Accelerate Program Power Supply
RSV	*	*	Reserved Pins
NC	*	*	No Connection

6. FUNCTIONAL DESCRIPTION

6.1 Interface Mode Selection and Description

This device can operate in two interface modes, one is Programmer interface mode, and the other is LPC interface mode. The Mode pin of the device provides the control between these two interface modes. These interface modes need to be configured before power up or return from #RESET. When ic (Mode) pin is set to V_{DD}, the device will be in the Programmer mode; while the Mode pin is set to low state (or leaved no connection), it will be in the LPC mode. In Programmer mode, this device just behaves like traditional flash parts with 8 data lines. But the row and column address inputs are multiplexed. The row address are mapped to the higher internal address A[18:11]. And the column address are mapped to the lower internal address A[10:0]. For LPC mode, it complies with the LPC Interface Specification, through the LAD[3:0] to communicate with the system chipset .

6.2 Read (Write) Mode

In Programmer interface mode, the read (write) operation of the W39V040B is controlled by #OE (#WE). The #OE (#WE) is held low for the host to obtain (write) data from (to) the outputs (inputs). #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when #OE is high. As for in the LPC interface mode, the read or write is determined by the "START CYCLE ". Refer to the LPC cycle definition and timing waveforms for further details.

6.3 Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is at low state, it will halt the device and all outputs will be at high impedance state. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals.

6.4 Boot Block Operation and Hardware Protection at Initial- #TBL & #WP

There is a hardware method to protect the top boot block and other sectors. Before power on programmer, tie the #TBL pin to low state and then the top boot block will not be programmed/erased. If #WP pin is tied to low state before power on, the other sectors will not be programmed/erased.

In order to detect whether the boot block feature is set on or not, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address 7FFF2(hex). You can check the DQ2/DQ3 at the address 7FFF2 to see whether the #TBL/#WP pin is in low or high state. If the DQ2 is “0”, it means the #TBL pin is tied to high state. In such condition, whether boot block can be programmed/erased or not will depend on software setting. On the other hand, if the DQ2 is “1”, it means the #TBL pin is tied to low state, then boot block is locked no matter how the software is set. Like the DQ2, the DQ3 inversely mirrors the #WP state. If the DQ3 is “0”, it means the #WP pin is in high state, then all the sectors except the boot block can be programmed/erased. On the other hand, if the DQ3 is “1”, then all the sectors except the boot block are programmed/erased inhibited.

To return to normal operation, perform a three-byte command sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

6.5 Sector Erase Command

Sector erase is a six-bus cycles operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the Sector erase command. The

Sector address (any address location within the desired Sector) is latched on the rising edge of R/#C in programmer mode, while the command (30H) is latched on the rising edge of #WE.

Sector erase does not require the user to program the device prior to erase. When erasing a Sector, the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic Sector erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last Sector erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

6.6 Program Operation

The W39V040B is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0." The erase operation, which changed entire data in main memory and/or boot block from "0" to "1", is needed before programming.

The program operation is initiated by a 4-byte command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (9μS typ. - T_{BP}) once it is completed and then return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

6.7 Hardware Data Protection

The integrity of the data stored in the W39V040B is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 5 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming and read operation are inhibited when V_{DD} is less than 2.0V typical.

(3) Write Inhibit Mode: Forcing #OE low or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

6.8 WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ5, DQ6, and DQ7. Each of DQ7 and DQ6 provides a method for determining whether a program or erase operation is complete or in progress. The device also offers a hardware-based output signal, RY/#BY in programmer mode, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: #Data Polling

The #Data Polling bit, DQ7, indicates whether an Embedded Program or Erase algorithm is in progress or completed. Data Polling is valid after the rising edge of the final #WE pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 and the complement of the data programmed to DQ7. Once the Embedded Program algorithm has completed, the device outputs the data programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, #Data Polling on DQ7 is active for about 1μS, and then the device returns to the read mode.

During the Embedded Erase algorithm, #Data Polling produces “0” on DQ7. Once the Embedded

Erase algorithm has completed, #Data Polling produces “1” on DQ7. An address within any of the sectors selected for erasure must be provided to read valid status information on DQ7.

Just before the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable (#OE) is set to low. That is, the device may change from providing status information to valid data on DQ7. Depending on when it samples the DQ7 output, the system may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ7-DQ0 will appear on successive read cycles.

RY/#BY: Ready/#Busy

The RY/#BY is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/#BY status is valid after the rising edge of the final #WE pulse in the command sequence. Since RY/#BY is an open-drain output, several RY/#BY pins can be tied together in parallel with a pull-up resistor to V_{DD}.

When the output is low (Busy), the device is actively erasing or programming. When the output is high (Ready), the device is in the read mode or standby mode.

DQ6: Toggle Bit

Toggle Bit on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final #WE pulse in the command sequence (before the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either #OE to control the read cycles. Once the operation has completed, DQ6 stops toggling.

The system can use DQ6 to determine whether a sector is actively erasing. If the device is actively erasing (i.e., the Embedded Erase algorithm is in progress), DQ6 toggles. If a program address falls within a protected sector, DQ6 toggles for about 1 μs after the program command sequence is written, and then returns to reading array data.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. DQ5 produces “1” under these conditions which indicates that the program or erase cycle was not successfully completed.

The device may output “1” on DQ5 if the system tries to program “1” to a location that was previously programmed to “0.” Only the erase operation can change “0” back to “1.” Under this condition, the device stops the operation, and while the timing limit has been exceeded, DQ5 produces “1.”

Under both these conditions, the system must write the reset command to return to the read mode.

Multi-Chip Operation

Multiple devices can be wired on the single LPC bus. There are four ID pins can be used to support up to 16 devices. But in order not to violate the BIOS ROM memory space defined by Intel, Winbond W39V040A will only used 3 ID pins to allow up to 8 devices, 4Mbytes for BIOS code and 4Mbytes for registers memory space.

7. REGISTER FOR LPC MODE

There are two kinds of registers on this device, the General Purpose Input Registers and Product Identification Registers. Users can access these registers through respective address in the 4Gbytes memory map. There are detail descriptions in the sections below.

7.1 General Purpose Inputs Register for LPC Mode

This register reads the FGPI[4:0] pins on the W39V040B.This is a pass-through register which can read via memory address FBC0100(hex). Since it is pass-through register, there is no default value.

GPI Register Table

BIT	FUNCTION
7 – 5	Reserved
4	Read FGPI4 pin status
3	Read FGPI3 pin status
2	Read FGPI2 pin status
1	Read FGPI1 pin status
0	Read FGPI0 pin status

7.2 Identification Input Pins ID[3:0]

These pins are part of mechanism that allows multiple parts to be used on the same bus. The boot device should be 0000b. And all the subsequent parts should use the up-count strapping. Note that a 1M byte ROM will occupy two Ids. For example: a 1MByte ROM's ID is 0000b, the next ROM's ID is 0010b. These pins all are pulled down with internal resistor.

7.3 Product Identification Registers

In the LPC interface mode, a read from FBC, 0000(hex) can output the manufacturer code, DA(hex). A read from FBC, 0001(hex) can output the device code 54(hex).

There is an alternative software method (six commands bytes) to read out the Product Identification in both the Programmer interface mode and the LPC interface mode. Thus, the programming equipment can automatically matches the device with its proper erase and programming algorithms.

In the software access mode, a six-byte (or JEDEC 3-byte) command sequence can be used to access the product ID for programmer interface mode. A read from address 0000(hex) outputs the manufacturer code, DA(hex). A read from address 0001(hex) outputs the device code, 54(hex). The product ID operation can be terminated by a three-byte command sequence or an alternate one-byte command sequence (see Command Definition table for detail).

8. TABLE OF OPERATING MODES

8.1 Operating Mode Selection - Programmer Mode

MODE	PINS				
	#OE	#WE	#RESET	ADDRESS	DQ.
Read	V_{IL}	V_{IH}	V_{IH}	AIN	Dout
Write	V_{IH}	V_{IL}	V_{IH}	AIN	Din
Standby	X	X	V_{IL}	X	High Z
Write Inhibit	V_{IL}	X	V_{IH}	X	High Z/DOUT
	X	V_{IH}	V_{IH}	X	High Z/DOUT
Output Disable	V_{IH}	X	V_{IH}	X	High Z

8.2 Operating Mode Selection - LPC Mode

Operation modes in LPC interface mode are determined by "START Cycle" when it is selected. When it is not selected, its outputs (LAD[3:0]) will be disable. Please reference to the "LPC Cycle Definition".

8.3 LPC Cycle Definition

FIELD	NO. OF CLOCKS	DESCRIPTION
Start	1	"0000b" appears on LPC bus to indicate the initial
Cycle Type & Dir	1	"010Xb" indicates memory read cycle; while "011xb" indicates memory write cycle. "X" mean don't have to care.
TAR	2	Turned Around Time
Addr.	8	Address Phase for Memory Cycle. LPC supports the 32 bits address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e. Address[31:28] on LAD[3:0] first , and Address[3:0] on LAD[3:0] last.)
Sync.	N	Synchronous to add wait state. "0000b" means Ready, "0101b" means Short Wait, "0110b" means Long Wait, "1001b" for DMA only, "1010b" means error, other values are reserved.
Data	2	Data Phase for Memory Cycle. The data transfer least significant nibble first and most significant nibble last. (i.e. DQ[3:0] on LAD[3:0] first, then DQ[7:4] on LAD[3:0] last.)

9. TABLE OF COMMAND DEFINITION

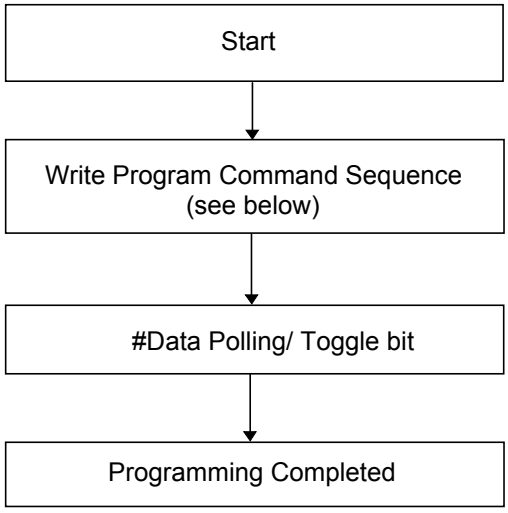
COMMAND DESCRIPTION	NO. OF Cycles (1)	1ST CYCLE Addr. Data	2ND CYCLE Addr. Data	3RD CYCLE Addr. Data	4TH CYCLE Addr. Data	5TH CYCLE Addr. Data	6TH CYCLE Addr. Data
Read	1	A_{IN} D_{OUT}					
Sector Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA(5) 30
Byte Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (4)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (4)	1	XXXX F0					

Notes:

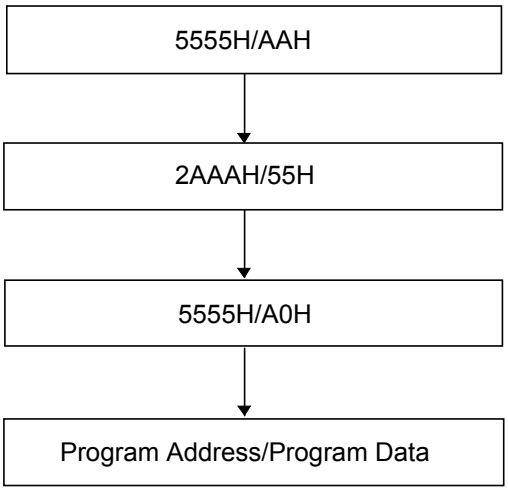
1. The cycle means the write command cycle not the LPC clock cycle.
2. The Column Address / Row Address are mapped to the Low / High order Internal Address. i.e. Column Address A[10:0] are mapped to the internal A[10:0], Row Address A[7:0] are mapped to the internal A[18:11]
3. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
4. Either one of the two Product ID Exit commands can be used.
5. SA: Sector Address

SA = 7XXXXh for Unique Sector7 (Boot Sector)	SA = 3XXXXh for Unique Sector3
SA = 6XXXXh for Unique Sector6	SA = 2XXXXh for Unique Sector2
SA = 5XXXXh for Unique Sector5	SA = 1XXXXh for Unique Sector1
SA = 4XXXXh for Unique Sector4	SA = 0XXXXh for Unique Sector0

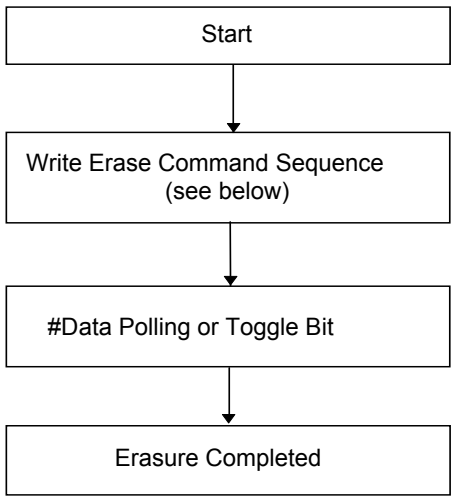
9.1 Embedded Programming Algorithm



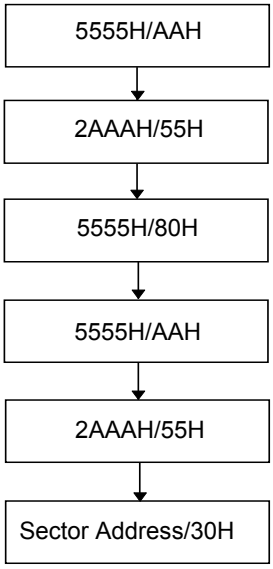
Program Command Sequence (Address/Command):



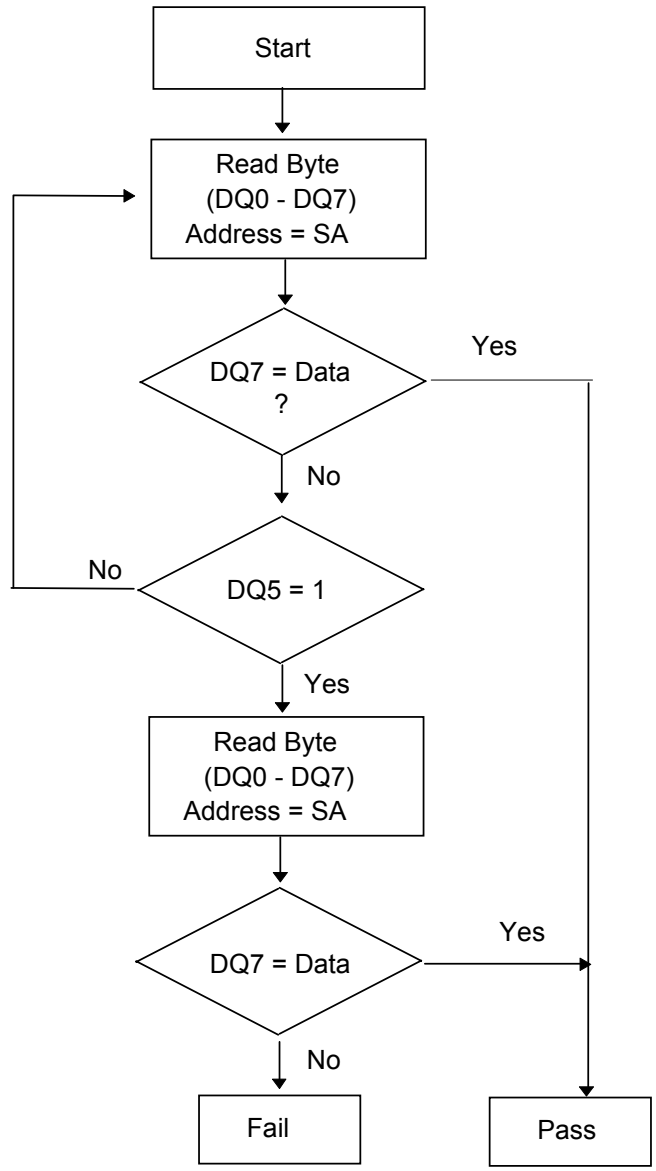
9.2 Embedded Erase Algorithm



Individual Sector Erase Command Sequence (Address/Command):

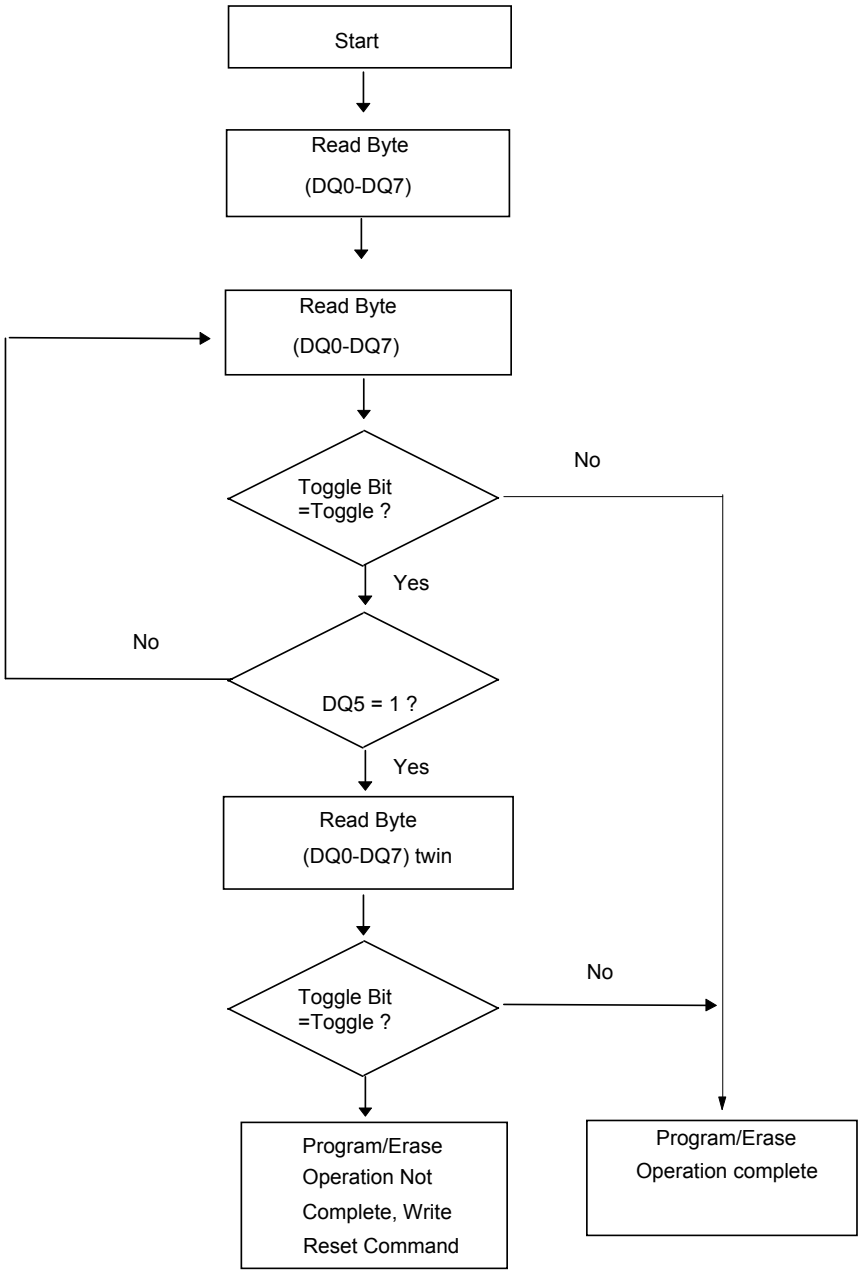


9.3 Embedded #Data Polling Algorithm



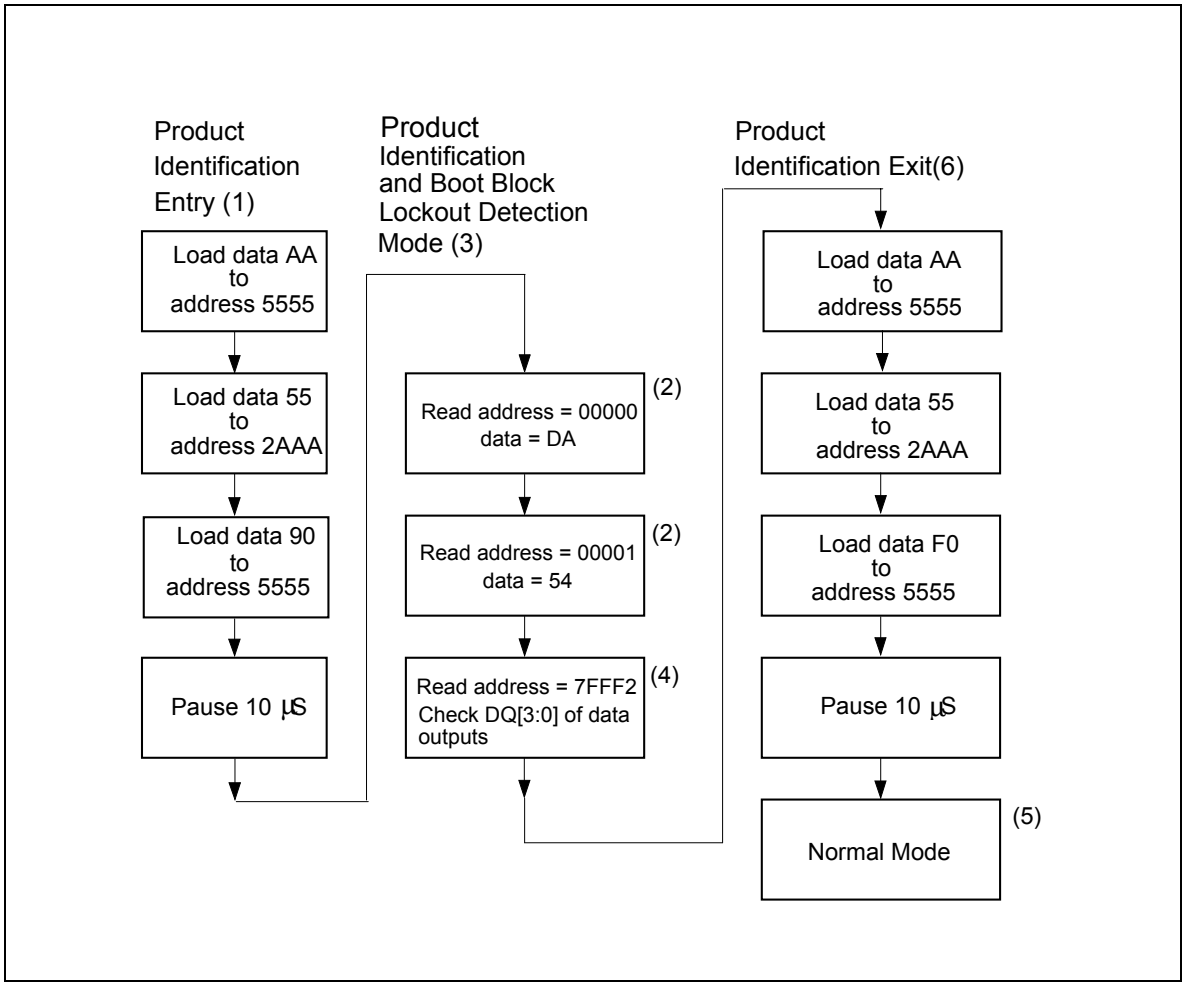
Note: SA = Valid address for programming .During a sector erase operation, a valid address is an address within any sector selected for erasure.

9.4 Embedded Toggle Bit Algorithm



Note: Recheck toggle bit because it may stop toggling as DQ5 changes to "1".

9.5 Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A18 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) The DQ[3:2] to indicate the sectors protect status as below:

	DQ2	DQ3
0	64Kbytes Boot Block Unlocked by #TBL hardware trapping	Whole Chip Unlocked by #WP hardware trapping Except Boot Block
1	64Kbytes Boot Block Locked by #TBL hardware trapping	Whole Chip Locked by #WP hardware trapping Except Boot Block

(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 (hex.) at XXXX address) can be used to exit the product identification/boot block lockout detection.

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.5 to V_{DD} +0.5	V
V_{PP} Voltage	-0.5 to +13	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +0.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings May adversely affect the life and reliability of the device.

10.2 Programmer interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	Icc	In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz	-	15	30	mA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	90	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	90	µA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	2.4	-	-	V

10.3 LPC Interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current Read	Icc	All I_{out} = 0A, CLK = 33 MHz, in LPC mode operation.	-	15	25	mA
Power Supply Current Program/Erase	Icc	CLK = 33 MHz, in LPC mode operation.	-	18	30	mA
Standby Current 1	Isb1	LPC4 = 0.9 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} / 0.1 V_{DD} no internal operation	-	20	50	uA
Standby Current 2	Isb2	LPC4 = 0.1 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} /0.1 V_{DD} no internal operation.	-	3	10	mA
Input Low Voltage	V_{IL}	-	-0.5	-	0.3 V_{DD}	V
Input Low Voltage of #INIT	V_{ILI}	-	-0.5	-	0.2 V_{DD}	V
Input High Voltage	V_{IH}	-	0.5 V_{DD}	-	V_{DD} +0.5	V
Input High Voltage of #INIT Pin	V_{IHI}	-	1.35 V	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA	-	-	0.1 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.9 V_{DD}	-	-	V

10.4 Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

10.5 Capacitance

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

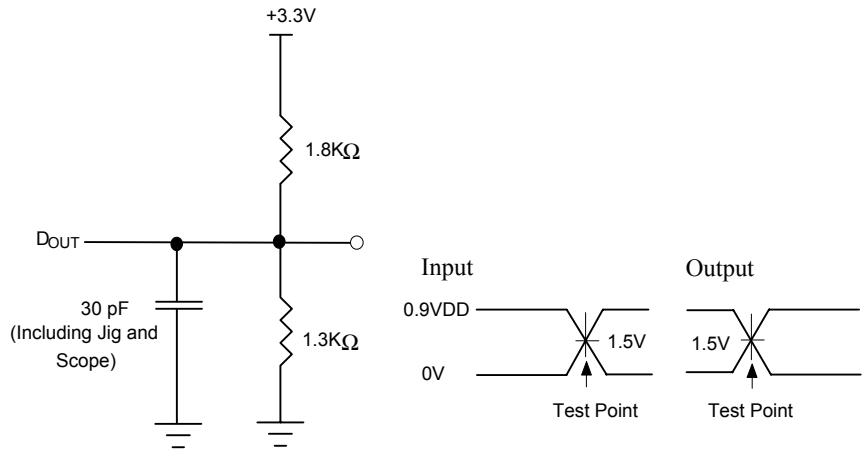
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

10.6 Programmer Interface Mode AC Characteristics

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 0.9 V_{DD}
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

AC Test Load and Waveform



Programmer Interface Mode AC Characteristics, continued

10.7 Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V040B		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	350	-	nS
Row / Column Address Set Up Time	T_{AS}	50	-	nS
Row / Column Address Hold Time	T_{AH}	50	-	nS
Address Access Time	T_{AA}	-	150	nS
Output Enable Access Time	T_{OE}	-	75	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#OE High to High-Z Output	T_{OHZ}	-	35	nS
Output Hold from Address Change	T_{OH}	0	-	nS

10.8 Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reset Time	T_{RST}	1	-	-	µS
Address Setup Time	T_{AS}	50	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
R/#C to Write Enable High Time	T_{CWH}	50	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	50	-	-	nS
#OE Hold Time	T_{OEH}	0	-	-	nS
Byte programming Time	T_{BP}	-	12	200	µS
Sector Erase Cycle Time (Note 2)	T_{PEC}	-	0.6	6	S
Program/Erase Valid to RY/#BY Delay	T_{BUSY}	90	-	-	nS

Notes: 1. All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low. Ref. to the AC testing condition.

2. Exclude 00H pre-program prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bytes are programmed to 00H before erasure

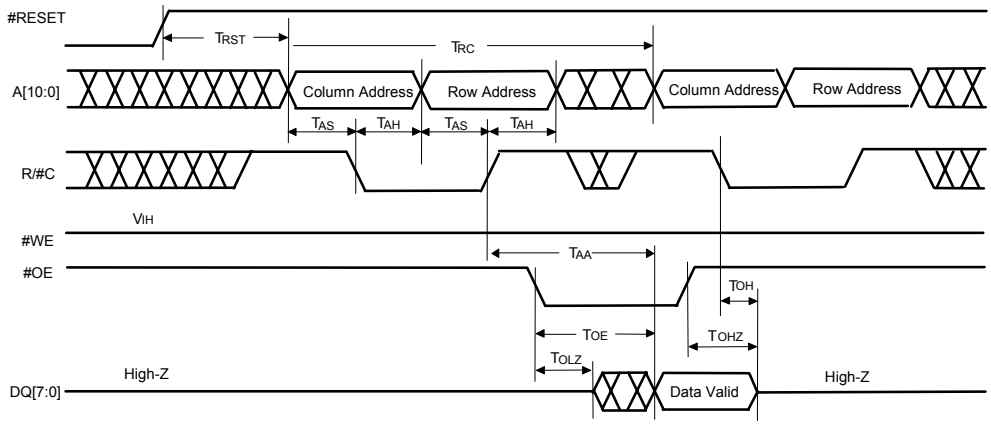
10.9 Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYMBOL	W39V040B		UNIT
		MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	350	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	350	nS
Toggle or Polling interval (for sector erase only) (Note1)	-	50	-	mS

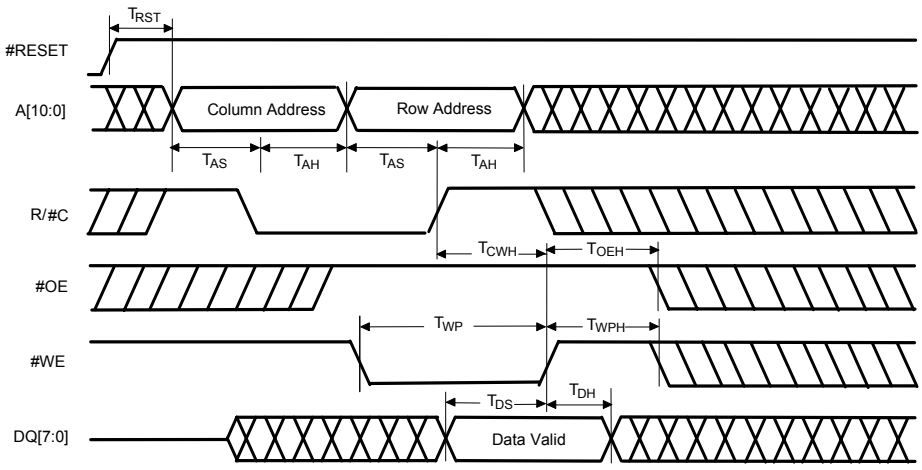
Note1: Minimum timing interval between Toggle-check or Polling-check is required for sector erase only

11. TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE

11.1 Read Cycle Timing Diagram

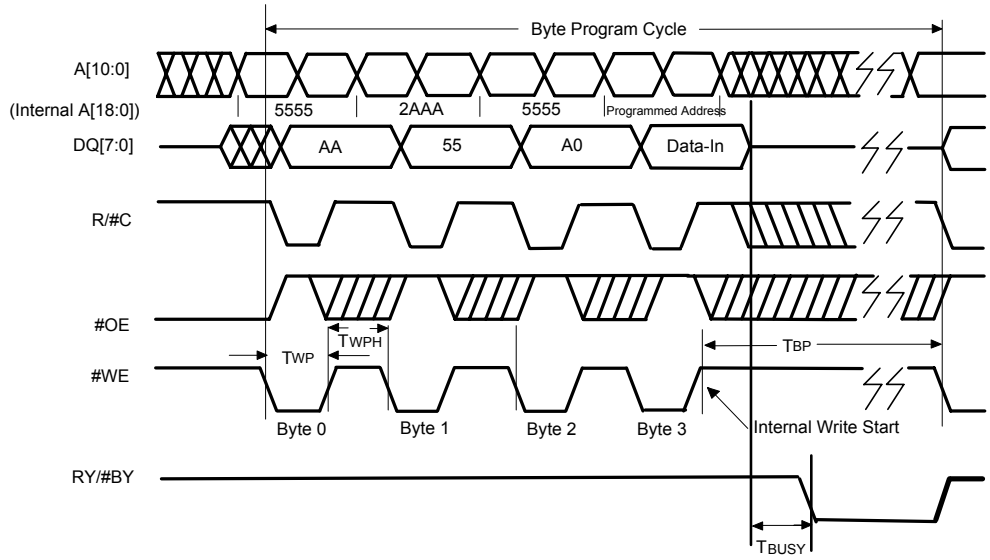


11.2 Write Cycle Timing Diagram



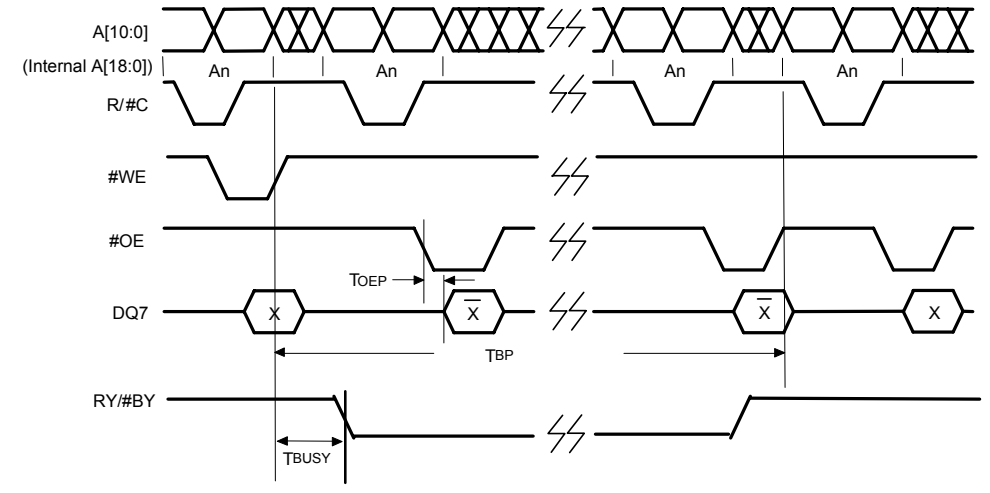
Timing Waveforms for Programmer Interface Mode, continued

11.3 Program Cycle Timing Diagram



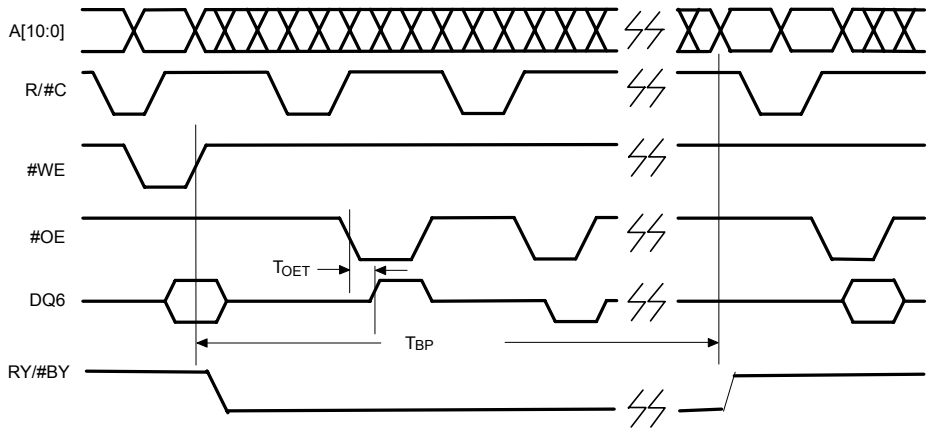
Note: The internal address A[18:0] are converted from external Column/Row address.
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[7:0] are mapped to the internal A[18:11].

11.4 #DATA Polling Timing Diagram

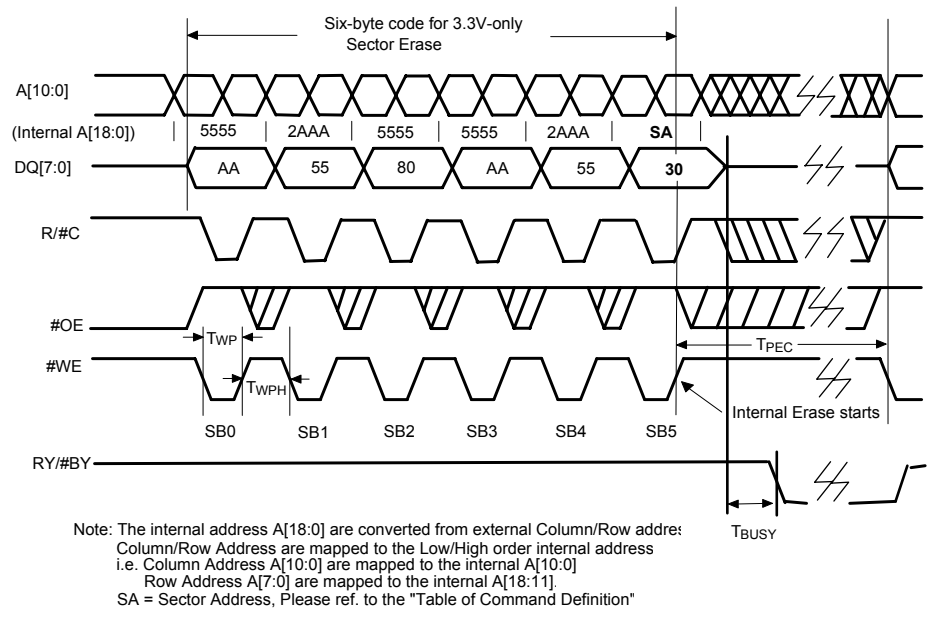


Timing Waveforms for Programmer Interface Mode, continued

11.5 Toggle Bit Timing Diagram



11.6 Sector Erase Timing Diagram



Note: The internal address A[18:0] are converted from external Column/Row addres
Column/Row Address are mapped to the Low/High order internal address
i.e. Column Address A[10:0] are mapped to the internal A[10:0]
Row Address A[7:0] are mapped to the internal A[18:11].
SA = Sector Address, Please ref. to the "Table of Command Definition"

12. LPC INTERFACE MODE AC CHARACTERISTICS

12.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6 V_{DD} to 0.2 V_{DD}
Input Rise/Fall Slew Rate	1 V/nS
Input/Output Timing Level	0.4V_{DD} / 0.4V_{DD}
Output Load	1 TTL Gate and C_L = 10 pF

12.2 Read/Write Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V040B		UNIT
		MIN.	MAX.	
Clock Cycle Time	T_{CYC}	30	-	nS
Input Set Up Time	T_{SU}	7	-	nS
Input Hold Time	T_{HD}	0	-	nS
Clock to Data Valid	T_{KQ}	2	11	nS

Note: Minimum and Maximum time have different load. Please refer to PCI specification.

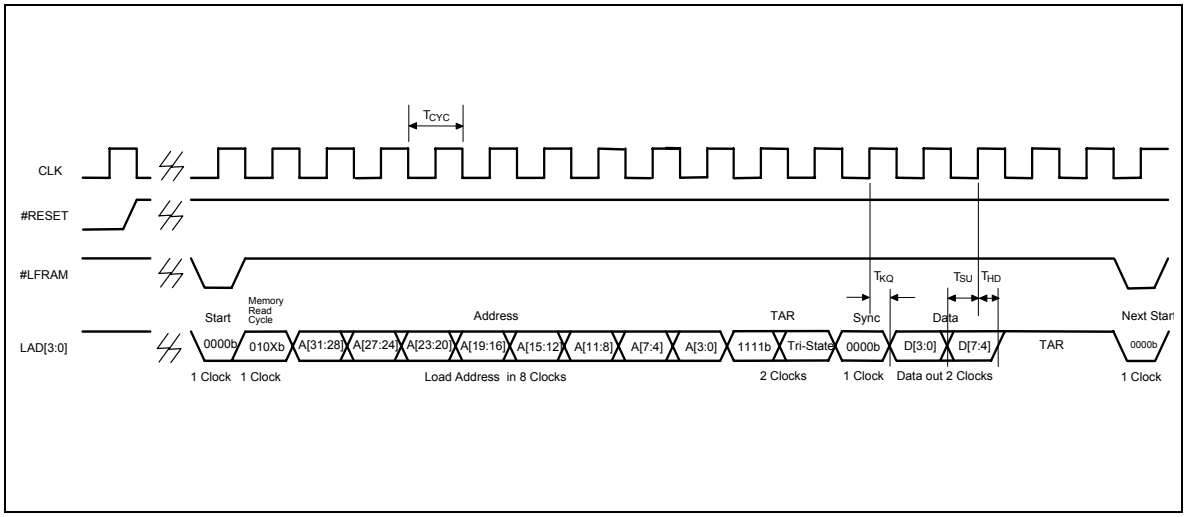
12.3 Reset Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{DD} stable to Reset Active	T_{PRST}	1	-	-	mS
Clock Stable to Reset Active	T_{KRST}	100	-	-	µS
Reset Pulse Width	T_{RSTP}	100	-	-	nS
Reset Active to Output Float	T_{RSTF}	-	-	50	nS
Reset Inactive to Input Active	T_{RST}	10	-	-	µS

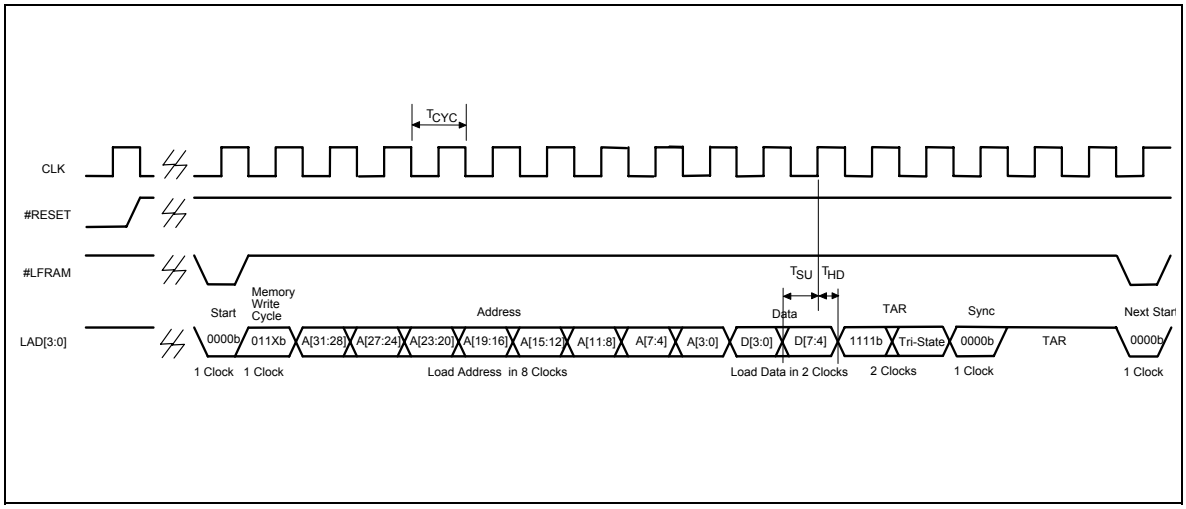
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.
Please refer to the AC testing condition.

13. TIMING WAVEFORMS FOR LPC INTERFACE MODE

13.1 Read Cycle Timing Diagram

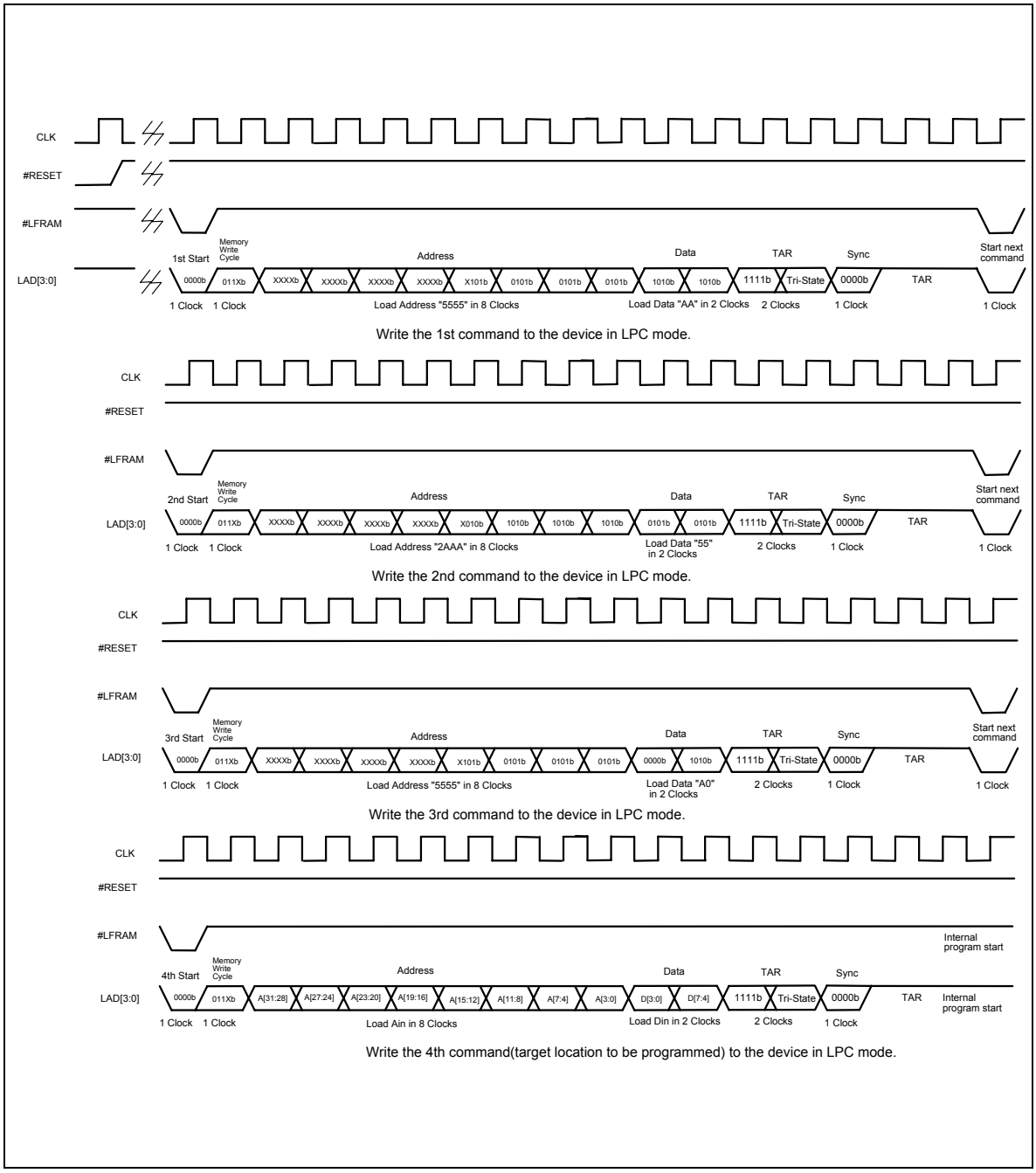


13.2 Write Cycle Timing Diagram



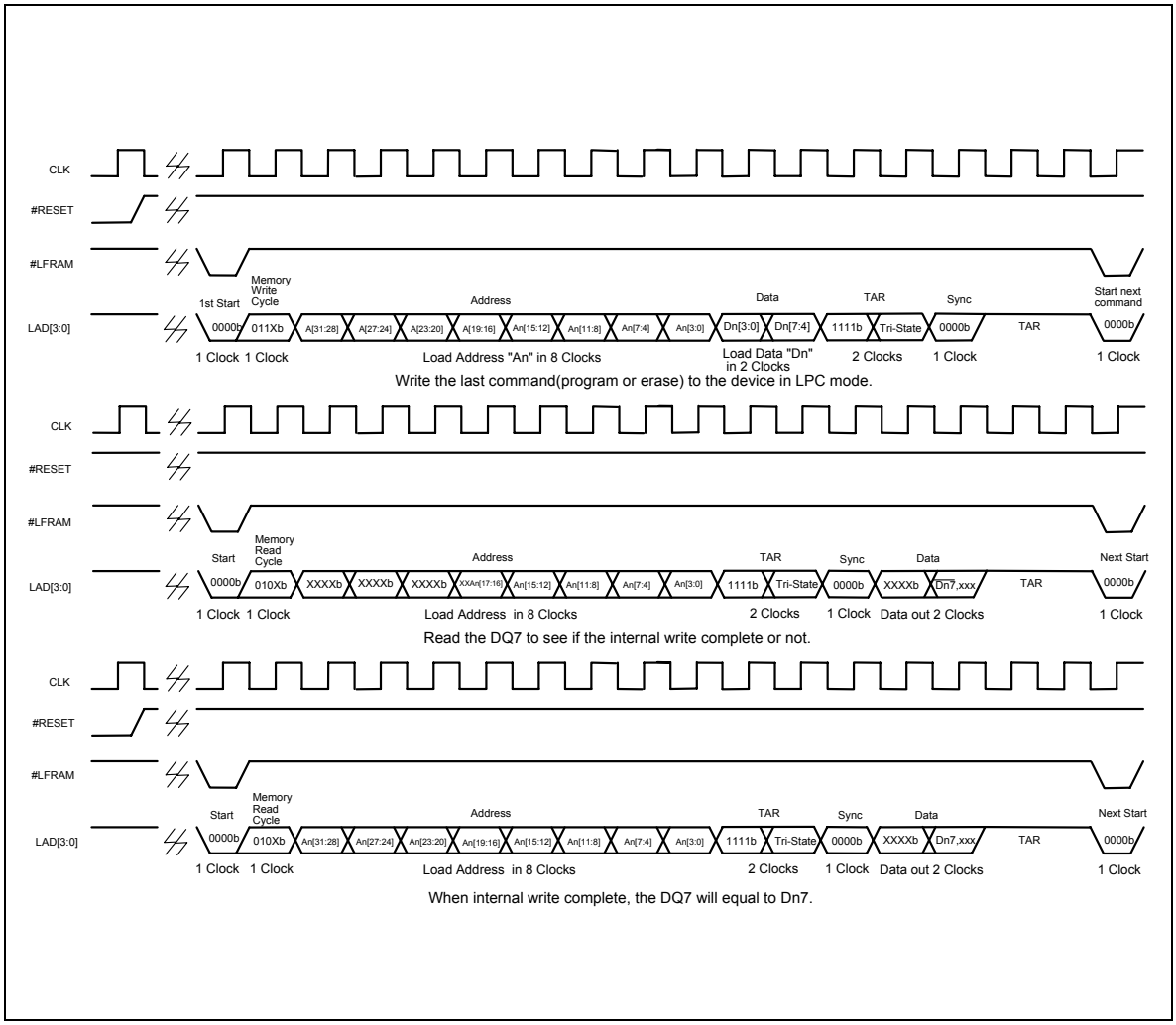
Timing Waveforms, for LPC Interface Mode, continued

13.3 Program Cycle Timing Diagram



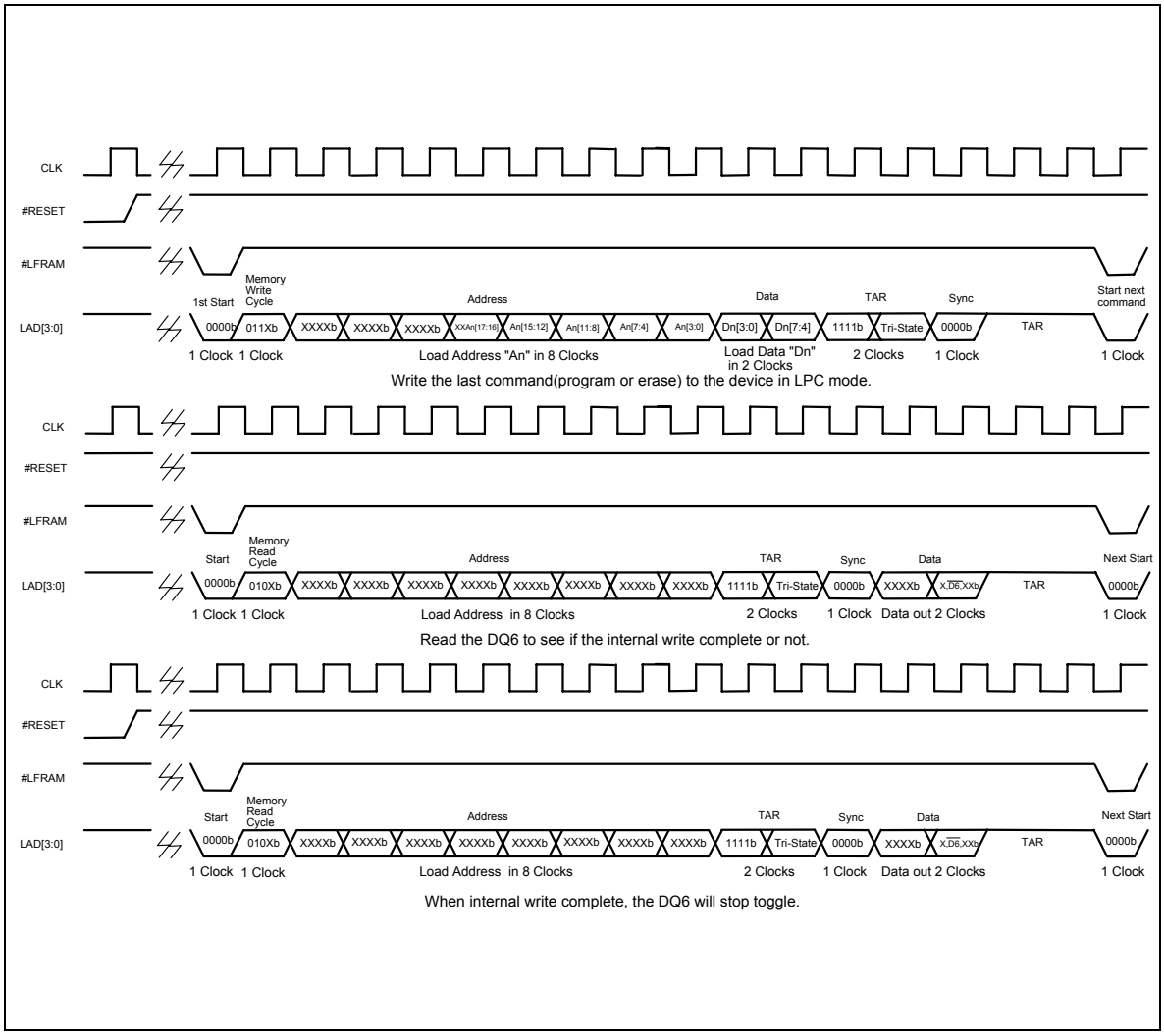
Timing Waveforms for LPC Interface Mode, continued

13.4 #DATA Polling Timing Diagram



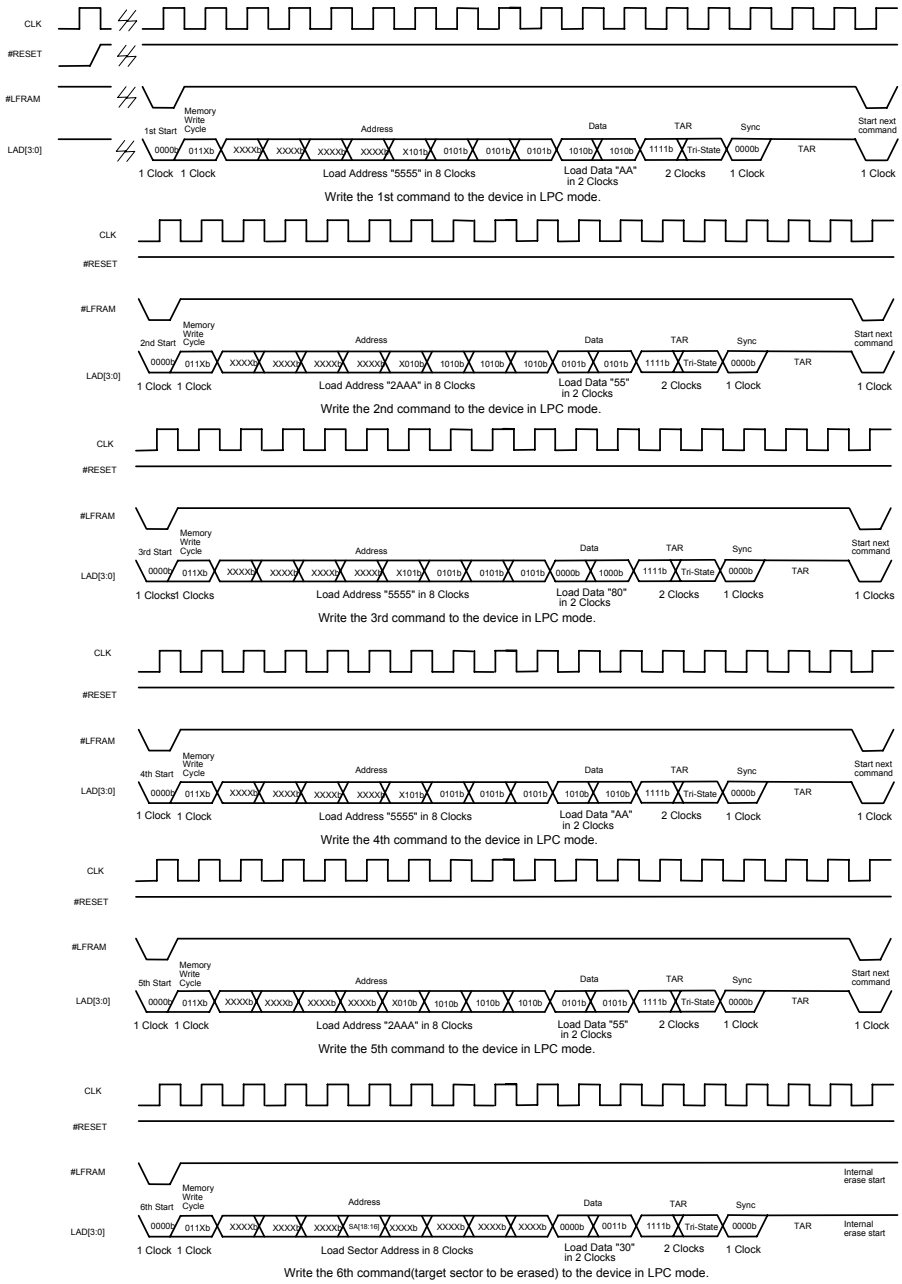
Timing Waveforms for LPC Interface Mode, continued

13.5 Toggle Bit Timing Diagram



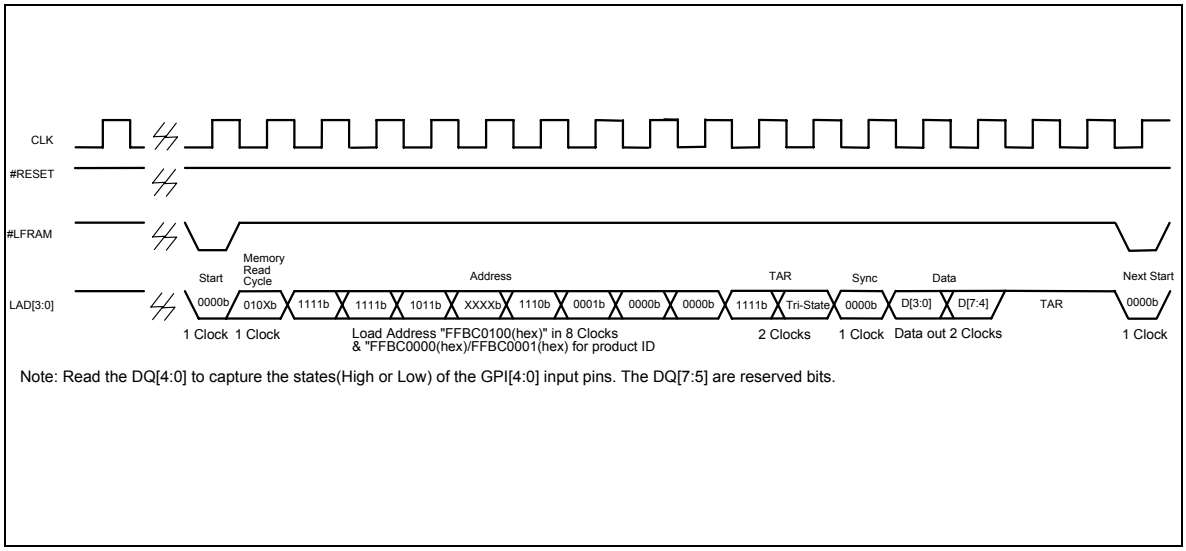
Timing Waveforms for LPC Interface Mode, continued

13.6 Sector Erase Timing Diagram



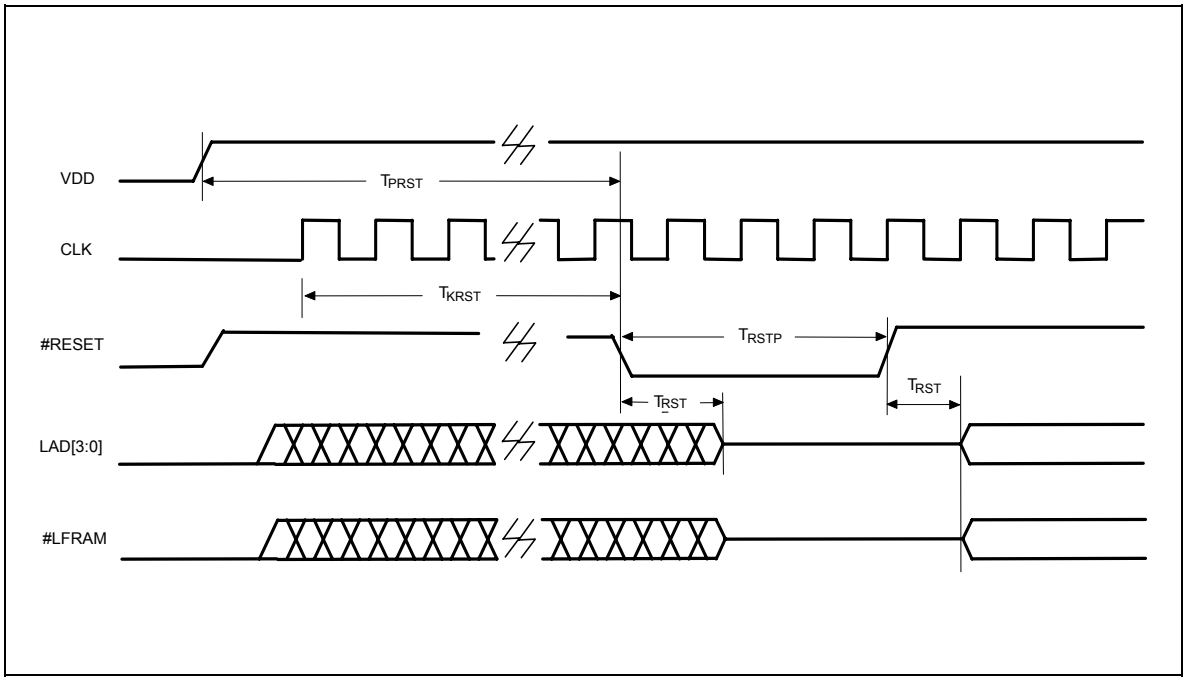
Timing Waveforms for LPC Interface Mode, continued

13.7 FGPI Register/Product ID Readout Timing Diagram



Note: Read the DQ[4:0] to capture the states(High or Low) of the GPI[4:0] input pins. The DQ[7:5] are reserved bits.

13.8 Reset Timing Diagram



14. ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (mA)	PACKAGE
W39V040BP	11	30	10	32L PLCC
W39V040BQ	11	30	10	32L STSOP
W39V040BPZ	11	30	10	32L PLCC Lead free
W39V040BQZ	11	30	10	32L STSOP Lead free

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

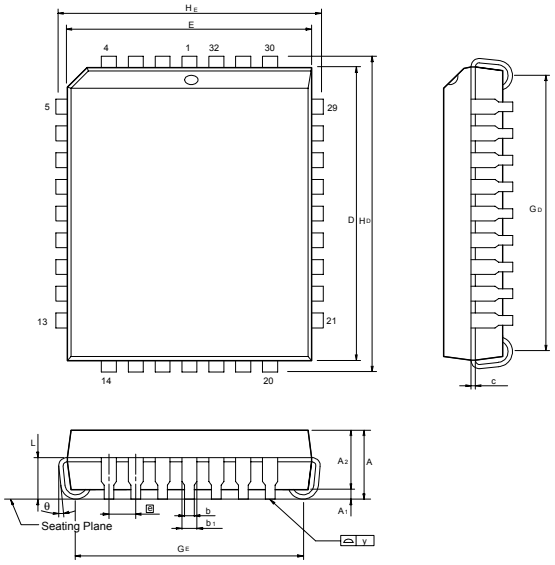
15. HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin STSOP W39V040BQZ

1st line: Winbond logo
2nd line: the part number: W39V040BQZ (Z: Lead free part)
3rd line: the lot number
4th line: the tracking code: 345 O B FA
149: Packages made in '03, week 45
O: Assembly house ID: A means ASE, O means OSE, ...etc.
B: ic revision; A means version A, B means version B, ...etc.
FA: Process code

16. PACKAGE DIMENSIONS

16.1 32L PLCC

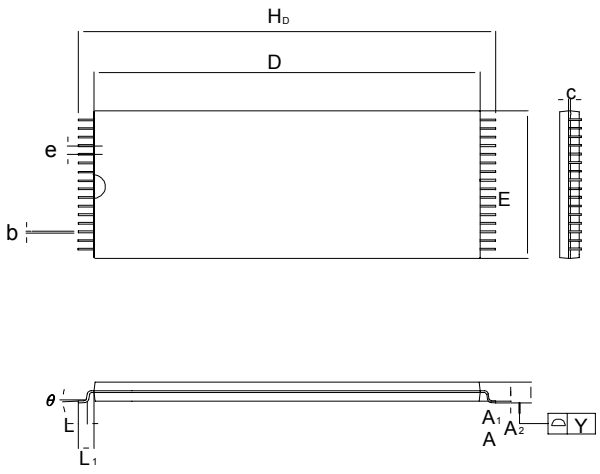


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusio
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

16.2 32L STSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0°	3°	5°	0°	3°	5°

17. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 26, 2004	-	Initial Issued
A2	Jan.25, 2005	P8, P9, P10	Delete 7.3 ~ 7.7 item Block lock relate description
A3	April 14, 2005	P32	Add important notice

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Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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